CLAIMS

What is claimed is:

1. A system comprising:

first and second modules, the first module having a first group of chips and the second module having a second group of chips;

a circuit board including first and second module connectors to receive the first and second modules, respectively;

a first buffer on the first module and a second buffer on the second module; and

a path including conductors in a first section that splits into a second section and third section, wherein the second section couples to the first buffer and the third section couples to the second buffer, and wherein the first buffer provides signals received from the second section to the first group of chips and the second buffer provides signals received from the third section to the second group of chips, and wherein impedances of the second and third sections are at least 50% greater than impedances of the first section.

2. The system of claim 1, wherein the impedances of the second and third sections are each greater than 60 ohms and the impedances of the first section are less than 40 ohms.

3. The system of claim 1, wherein the first module includes terminations for the path including the first and second sections and the first buffer is in parallel with the terminations.

4. The system of claim 3, wherein the terminations each have impedances that are at least 50% greater than the impedances of the first section.

5. The system of claim 4, wherein the impedances of the terminations are each greater than 60 ohms and the impedances of the first section are less than 40 ohms.

6. The system of claim 1, wherein the first module includes first terminations for the path including the first and second sections and the first buffer is in parallel with the first terminations, and the second module includes second terminations for the path including the first and third sections and the second buffer is in parallel with the second terminations.

7. The system of claim 1, wherein the first and second buffers each have impedances that are at least 50% greater than the impedances of the first section.

8. The system of claim 1, wherein the first buffer includes terminations for the path including the first and second sections and the second buffer includes terminations for the path including the first and third sections.

9. The system of claim 1, wherein the first buffer provides signals received from the second section to the first group of chips and the second buffer provides signals received from the third section to the second group of chips.

10. The system of claim 9, wherein the signals include address and command signals.

11. A system comprising:

first and second modules, the first module having a first group of chips and the second module having a second group of chips;

a circuit board including first and second module connectors to receive the first and second modules, respectively;

a first buffer on the first module and a second buffer on the second module;

a path including conductors in a first section that splits into a second section and third section, wherein the second section couples to the first buffer and the third section couples to the second buffer; and

wherein the first buffer includes on die terminations for the path including the first and second sections, and the second buffer includes on die terminations for the path including the first and third sections.

12. The system of claim 11, wherein impedances of the second and third sections are at least 50% greater than impedances of the first section.

13. The system of claim 11, wherein impedances of the second and third sections are each greater than 60 ohms and impedances of the first section are less than 40 ohms.

14. The system of claim 11, wherein the first buffer provides signals received from the second section to the first group of chips and the second buffer provides signals received from the third section to the second group of chips.

15. The system of claim 11, wherein the signals include address and command signals.

16. A system comprising:

first and second modules, the first module having a first group of chips and the second module having a second group of chips;

a circuit board including first and second module connectors to receive the first and second modules, respectively;

a first buffer on the first module and a second buffer on the second module;

a path including conductors in a first section that splits into a second section and third section, wherein the second section couples to the first buffer and the third section couples to the second buffer; and

wherein the first module includes first terminations for the path including the first and second sections and the first buffer is in parallel with the first terminations, and the second module includes second terminations for the path including the first and third sections and the second buffer is in parallel with the second terminations.

17. The system of claim 16, wherein the impedances of the second and third sections are each greater than 60 ohms and the impedances of the first section are less than 40 ohms.

18. The system of claim 16, wherein the first and second terminations each have impedances that are at least 50% greater than the impedances of the first section.

19. The system of claim 16, wherein the impedances of the first and second terminations are each greater than 60 ohms and the impedances of the first section are less than 40 ohms.

20. The system of claim 16, wherein the first module includes first terminations for the path including the first and second sections and the first buffer is in parallel with the terminations, and the second module includes second terminations for the path including the first and third sections and the second buffer is in parallel with the second terminations.

21. The system of claim 16, wherein the first buffer provides signals received from the second section to the first group of chips and the second buffer provides signals received from the third section to the second group of chips.

22. The system of claim 16, wherein the signals include address and command signals.

23. The system of claim 16, wherein the circuit board is a printed circuit board and a motherboard.